ABSTRACT

A system and method for generating a boundary-scan description language file is disclosed. In a simplified embodiment of the invention, the system utilizes a memory; software stored within the memory defining functions to be performed by the system; and a processor. The processor is configured by the software to: create a flat netlist that describes the integrated circuit, wherein the flat netlist comprises connectivity information regarding leaf cells within the integrated circuit; determine and store a name provided for each joint test action group register located within the integrated circuit, from the created flat netlist; determine relationships between each joint test action group register located within the integrated circuit and at least one input/output pin located within the integrated circuit, from the created flat netlist, and store a description of the relationships; and create a boundary-scan description language file from the stored names of each joint test action group and the stored description of the relationship between the joint test action group register and the input/output pin.